# CIRCUITRY FOR REDUCING LEAKAGE CURRENTS IN A TRANSMISSION GATE SWITCH USING VERY SMALL MOSFET DEVICES

## ABSTRACT OF THE DISCLOSURE

A test circuit for connecting a high-impedance node to an external test point when a test signal is enabled. The test circuit comprises: a first transmission gate switch for coupling the high impedance node to a first internal node of the test circuit when the test signal is enabled, the first transmission gate switch comprising a first N-channel transistor having a drain coupled to the high impedance node, a gate coupled to a Logic 1 when the test signal is enabled, and a source coupled to the first internal node. The test circuit also comprises a second transmission gate switch capable of coupling the first internal node to the external test point when the test signal is enabled and a biasing circuit for generating a negative Vgs bias on the first N-channel transistor when the test signal is disabled to thereby reduce leakage current in the first N-channel transistor.